Remarks

Applicants respectfully request reconsideration of this application as amended. Claims 15 and 27 have been amended. No claims have been cancelled. Therefore, claims 1, 2, 6, 12-16 and 21-32 are presented for examination.

Claim 27 stands rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Applicants submit that this rejection has been obviated by amendment of claim 27.

Claims 1, 2, 6, 12-16, 21 and 24-27, 29-32 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kamiya (U.S. Patent No. 5,809,335) in further view of the applicant admitted prior art (AAPA). Applicants submit that the present claims are patentable over any combination of Kamiya and the APA.

Kamiya discloses a method and a data transfer apparatus capable of handling DMA block transfer interruptions. See Kamiya at Abstract. The data transfer apparatus includes a plurality of direct memory access (DMA) channels each having different priorities and at least one backup channel information memory for saving control information necessary for a restart of an interrupted DMA transfer through one of the DMA channels. The data transfer apparatus further includes a control means responsive to transfer commands, which command DMA transfers through the DMA channels. Id. In addition, the control means executes various interrupt handling steps when a transfer command interrupts an execution of a DMA transfer through one of the DMA channels having a lower priority than the priority of the DMA channel used by the interrupting transfer command, so that an interruption of an important data transfer can be prevented. Id.

The APA rejection is based upon applicants' background section in the specification. The background section discloses an I/O device coupled to a DMA channel. See Specification at Fig. 4A and page 2, line 13 – page 3, line 8. Nevertheless,

applicants background section does not disclose or suggest a DMA controller that terminates a DMA transfer before a terminal count is reached upon receiving a retransmit request signal from the I/O device, or a DMA controller that re-executes a DMA transfer with an I/O device upon receiving a request from the I/O device.

Claim 1 recites an input/output (I/O) device coupled to the DMA controller, wherein the DMA controller terminates a DMA transfer before a terminal count is reached upon receiving an early termination request signal from the I/O device. Applicants submit that neither Kamiya, nor the APA disclose or suggest a DMA controller that terminates a DMA transfer before a terminal count is reached upon receiving an early termination request signal from the I/O device.

Kamiya discloses that a first DMA transfer is interrupted when a command for a second DMA transfer through a DMA channel with a higher priority than the current DMA channel is issued during the first DMA transfer. As a result, values for the current DMA channel are transferred to a backup channel information memory and saved. Subsequently a second DMA transfer involving the higher priority channel is carried out. Afterwards, the first DMA block transfer is restarted based on the saved values. See Kamiya at col. 4, ll. 56 – col. 5, ll. 6. Applicants submit that the **interruption and resumption** of a DMA transfer is not equivalent to the **termination** of a DMA transfer. Accordingly, claim 1 is patentable over Kamiya in view of the admitted prior art.

Claim 12 recites an input/output (I/O) device coupled to a DMA controller, wherein the DMA controller re-executes a DMA transfer with the I/O device upon receiving a retransmit request signal from the I/O device. Kamiya does not disclose or suggest a DMA controller that re-executes a data transfer upon receiving a request from

an I/O device. As discussed above, Kamiya discloses the interruption and resumption of a DMA transfer, not re-executing a transfer.

Further, the APA does not disclose or suggest a DMA controller that re-executes a data transfer upon receiving a request from an I/O device. Since neither Kamiya nor the APA disclose or suggest DMA controller re-executes a DMA transfer with the I/O device upon receiving a retransmit request signal from the I/O device, any combination of Kamiya and the APA would also fail to disclose or suggest such a limitation. Therefore, claim 12 is patentable over Kamiya in view of the APA. Claims 29-32 depend from claim 12 and include additional limitations. Therefore, claims 29-32 are also patentable over Kamiya in view of the APA.

Claim 13 recites receiving a request signal at a DMA controller from a first device indicating a request by the first device to re-transmit the data between the first device and a second device, and re-transferring the data between the first device and the second device. For the reasons described above with respect to claim 12, claim 13 is also patentable over Kamiya in view of the APA. Because claims 14 depends from claim 13 and includes additional limitations, claim 14 is also patentable over Kamiya in view of the APA.

Claim 15 recites receiving a request signal at a DMA controller from a first device indicating a request by the first device to terminate a transfer of data between the first device and a second device, and terminating the transfer of data between the first device and the second device. For the reasons described above with respect to claim 1, claim 15 is also patentable over Kamiya in view of the APA. Since claims 16, and 21-23 depend

from claim 15 and include additional limitations, claims 16, and 21-23 are also patentable over Kamiya in view of the APA.

Claim 22 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Kamiya (U.S. Patent No. 5,809,335) and the application admitted prior art (APA) as applied to claims 1, 2, 6, 12-16, 21 and 24-32, and further in view of Murray (U.S. Patent No. 5,903,775). Applicants submit that the present claims are patentable over any Kamiya and the APA even in view of Murray.

Murray discloses a method for allowing the transmission of digital video segments along a number of transmission channels. See Murray at Abstract. Nevertheless, Murray does not disclose or suggest an input/output (I/O) device coupled to a DMA controller, wherein the DMA controller terminates a DMA transfer before a terminal count is reached upon receiving an early termination request signal from the I/O device. In addition, Murray does not disclose or suggest a DMA controller that re-executes a data transfer upon receiving a request from an I/O device.

As previously discussed, Kamiya and the APA do not disclose or suggest the above features. Therefore, any combination of Kamiya, the APA and Murray also would not disclose or suggest an input/output (I/O) device coupled to a DMA controller, wherein the DMA controller terminates a DMA transfer before a terminal count is reached upon receiving an early termination request signal from the I/O device, or a DMA controller that re-executes a data transfer upon receiving a request from an I/O device. Accordingly, the present claims are patentable over Kamiya in view of the APA and further in view of Murray.

Applicants respectfully submit that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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